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VANJ 2022

Ultra-Low-Power (ULP) System-on-Chip (SoC) for Internet-of-Things (IoT) Edge Computing

Trong-Thuc Hoang

2022/11

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Outline

1. Introduction
2. Ultra-low-power SoC state-of-the-art
3. Our attempt for Ultra-low-power SoC
4. Conclusion

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1. Introduction (1/3) Author

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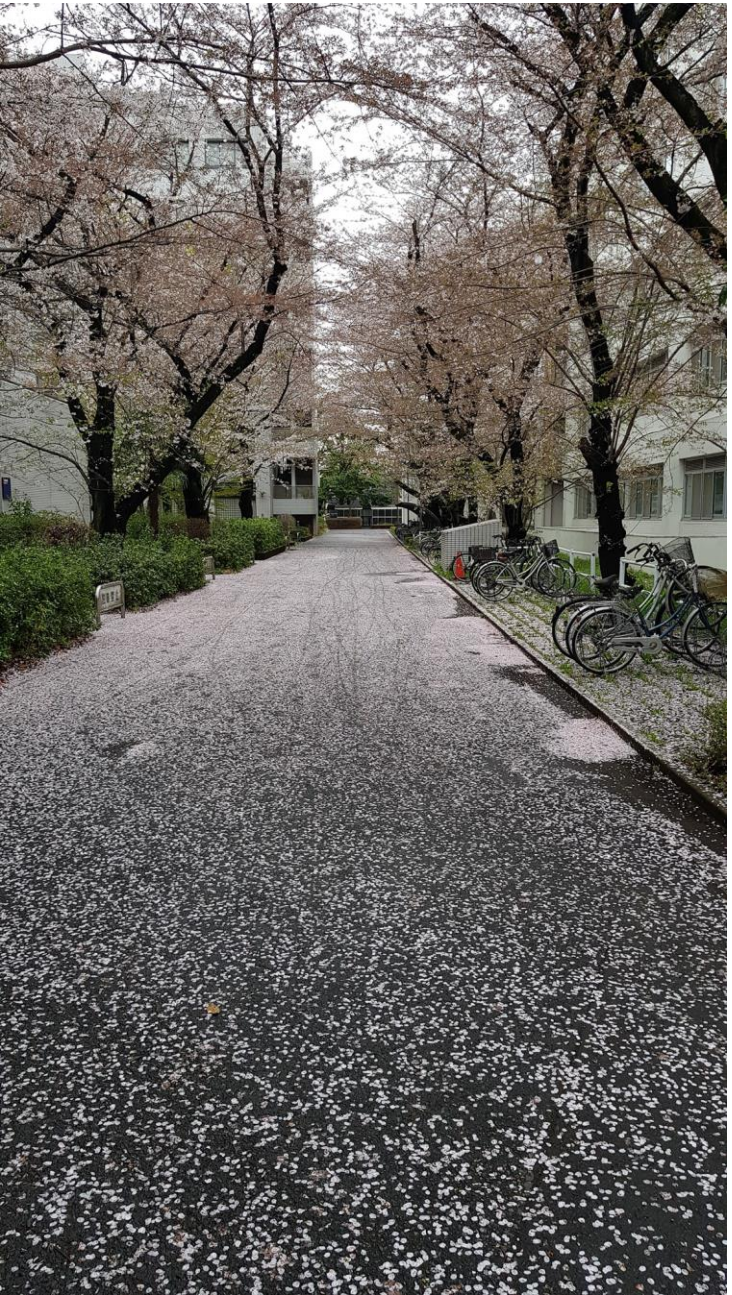
https://thuchoang90.github.io/

(you can find tutorials and project sources on the website)

1. Introduction (2/3) University



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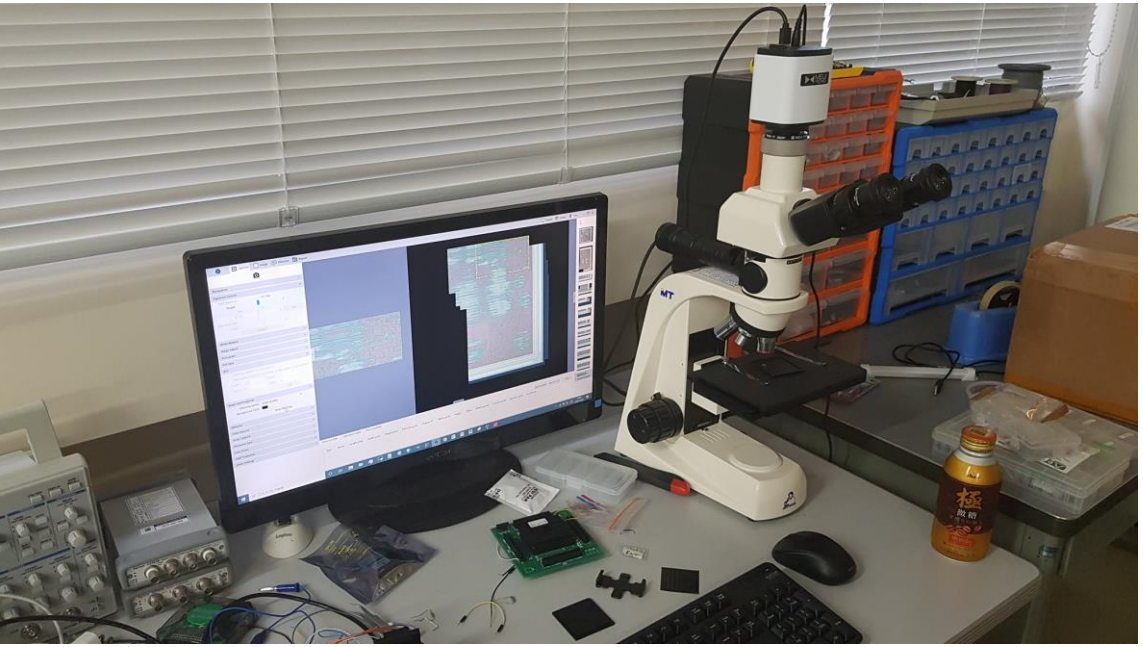
University of Electro-Communications (UEC), Tokyo, Japan

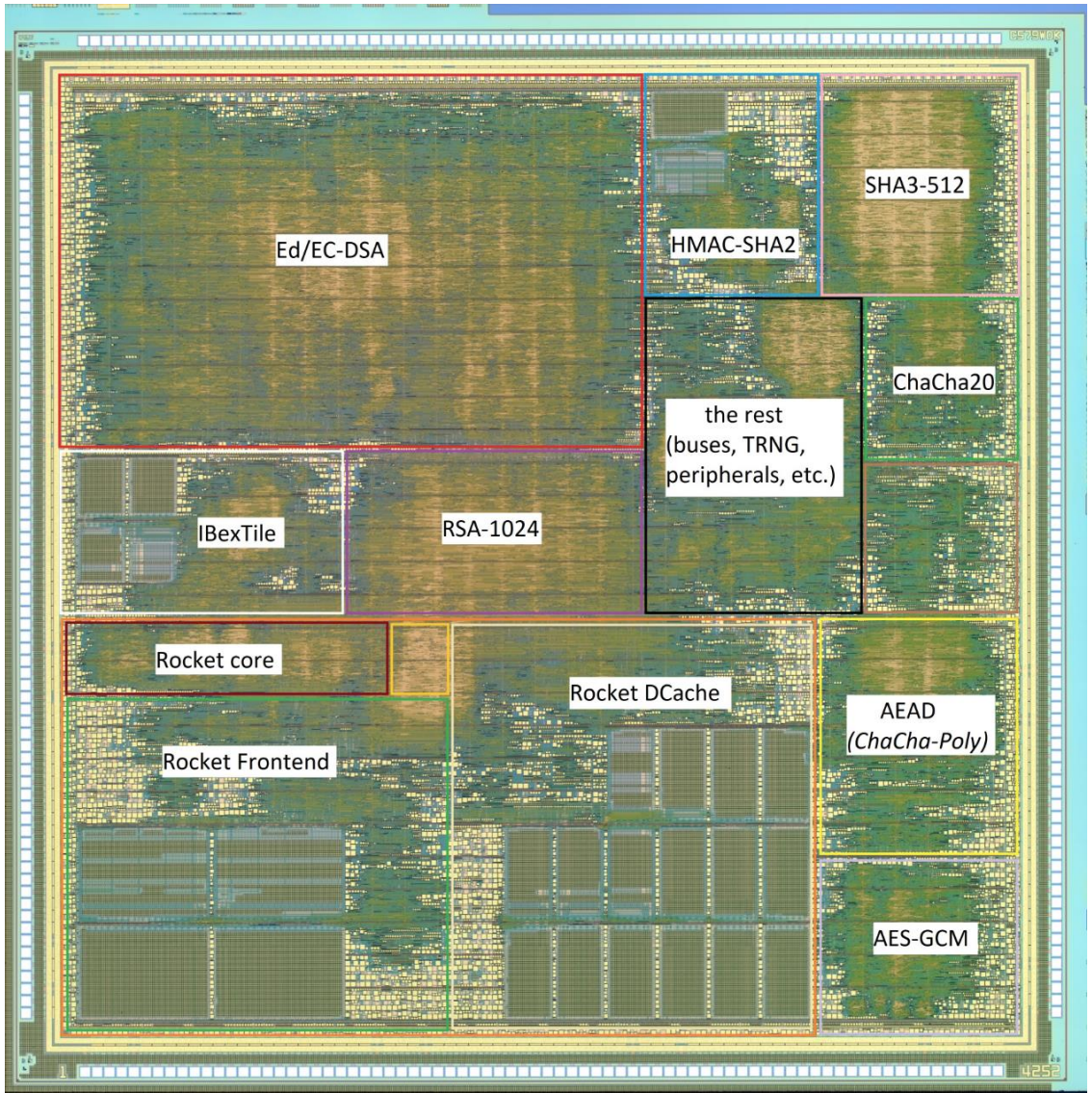
https://www.uec.ac.jp/

1. Introduction (3/3) Laboratory



http://vlsilab.ee.uec.ac.jp/

Pham Laboratory
Integrated circuit design laboratory



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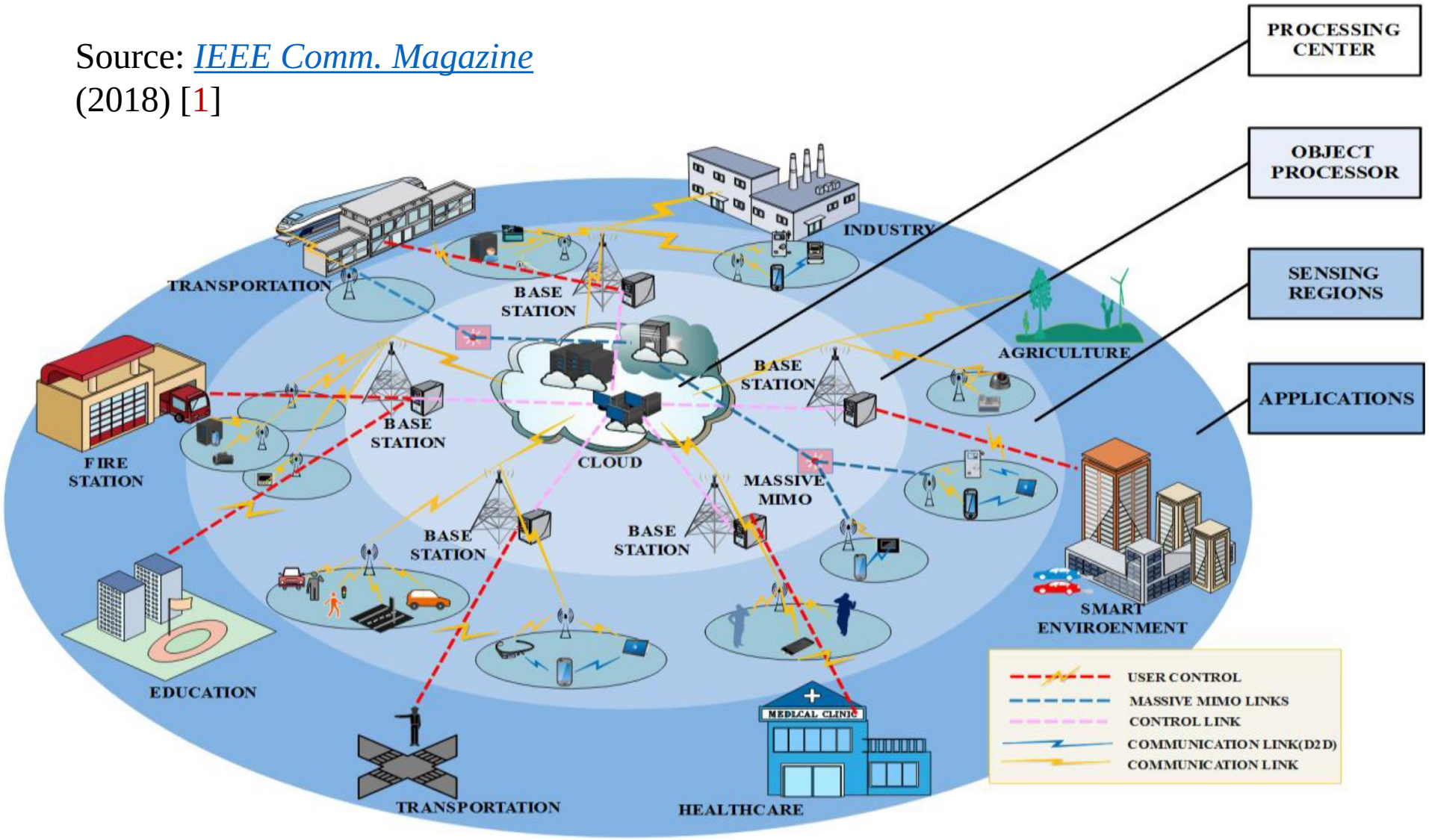
2. Ultra-low-power SoC (1/8) Needs for IoT edge

Source: *IEEE Comm. Magazine* (2018) [1]

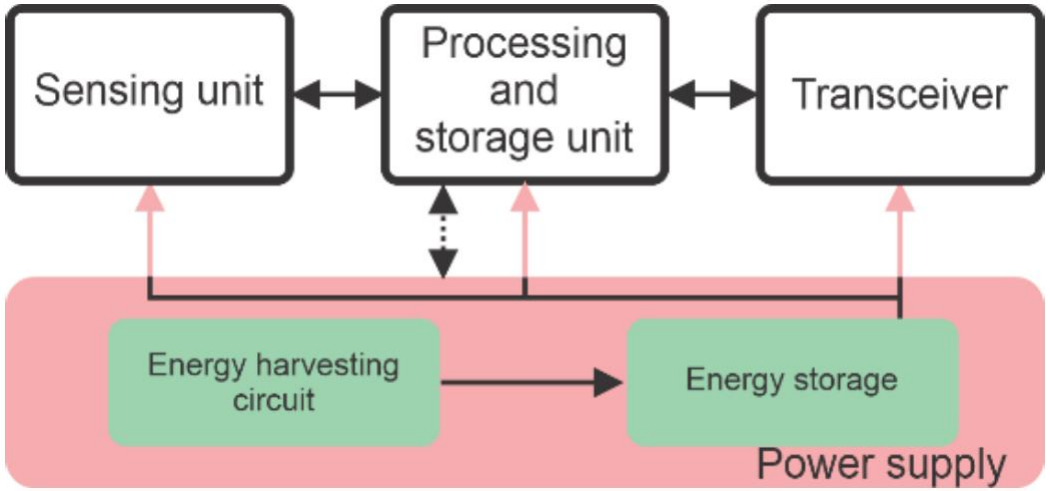


- **IoT:** *a massive network of heterogeneous and ubiquitous objects*
- **Consists of:**
  - ❑ Cloud computing: *data centers & servers*
  - ❑ Fog computing: *routers & gateways*
  - ❑ Edge computing: *application devices*

2. Ultra-low-power SoC (2/8) Typical IoT edge node

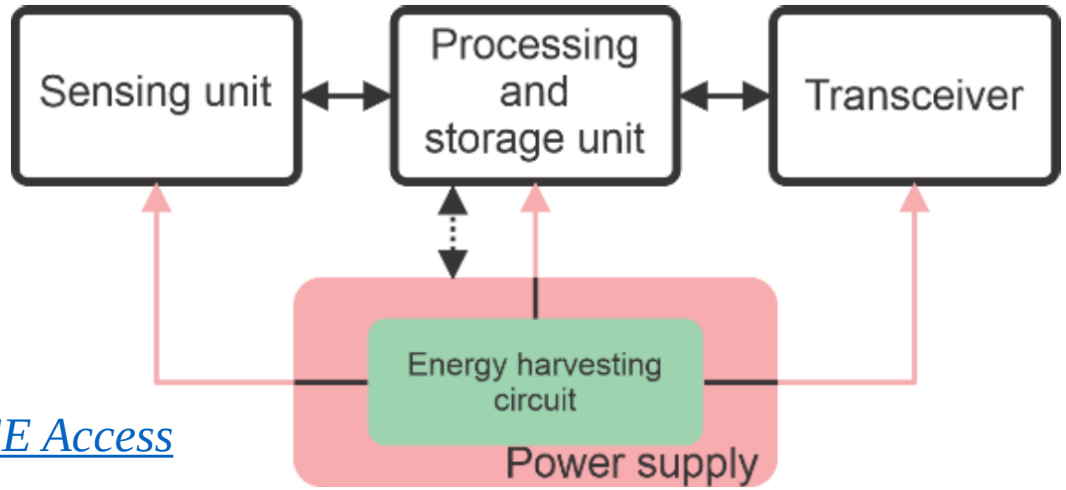
A typical IoT edge node nowadays:

- Sensor
- MCU *(+memory)*
- Transceiver
- Power supply *(+energy harvesting)*



Battery IoT node

Source: *IEEE Access* (2021) [2]



Battery-less IoT node

Lower the power consumption of the MCUs
→ Pushing more computational capability to the IoT nodes
→ Data can be processed locally *(rather than sent frequently to the cloud)*
→ Reduce responding latency *AND* transceiver's energy
(given the fact that RF modules nowadays consume more than the MCUs)

2. Ultra-low-power SoC (3/8) Energy harvesting today

Energy source	Technology	Power density	Advantages	Disadvantages
Solar	PV cell	10 - 100 mW / cm^2 (outdoor) < 100 µW / cm^2 (indoor)	High-output voltage Low fabrication costs Predictable	Unavailable at night Non-controllable
RF	Antenna	0.01 - 0.1 µW / cm^2 1- 10 mW / cm^2	Available anywhere, anytime Predictable Controllable	Distance dependent Low-power density
Mechanical vibrations and pressure	Piezoelectric	4 - 250 µW / cm^3	High-power density No external voltage source Simplicity design and fabrication Controllable	Highly variable output Unpredictable
	Electromagnetic	300 - 800 µW / cm^3	High-output currents Robustness Low-cost design Controllable	Relatively large size Unpredictable
	Electrostatic	50 – 100 µW / cm^3	High-output voltage Relatively larger output power density Possibility to build low-cost devices Controllable	Requires bias voltage Unpredictable
Human heat	Piezoelectric Pyroelectric	< 35 µW / cm^2	Sustainable and reliable Available Controllable	Low-power density Unpredictable
Biomechanical	Electromagnetic Piezoelectric Triboelectric Electrostatic	< 4 µW / cm^3 < 300 µW / cm^3	Available Controllable	Low-power density Unpredictable

Energy harvesting nowadays:

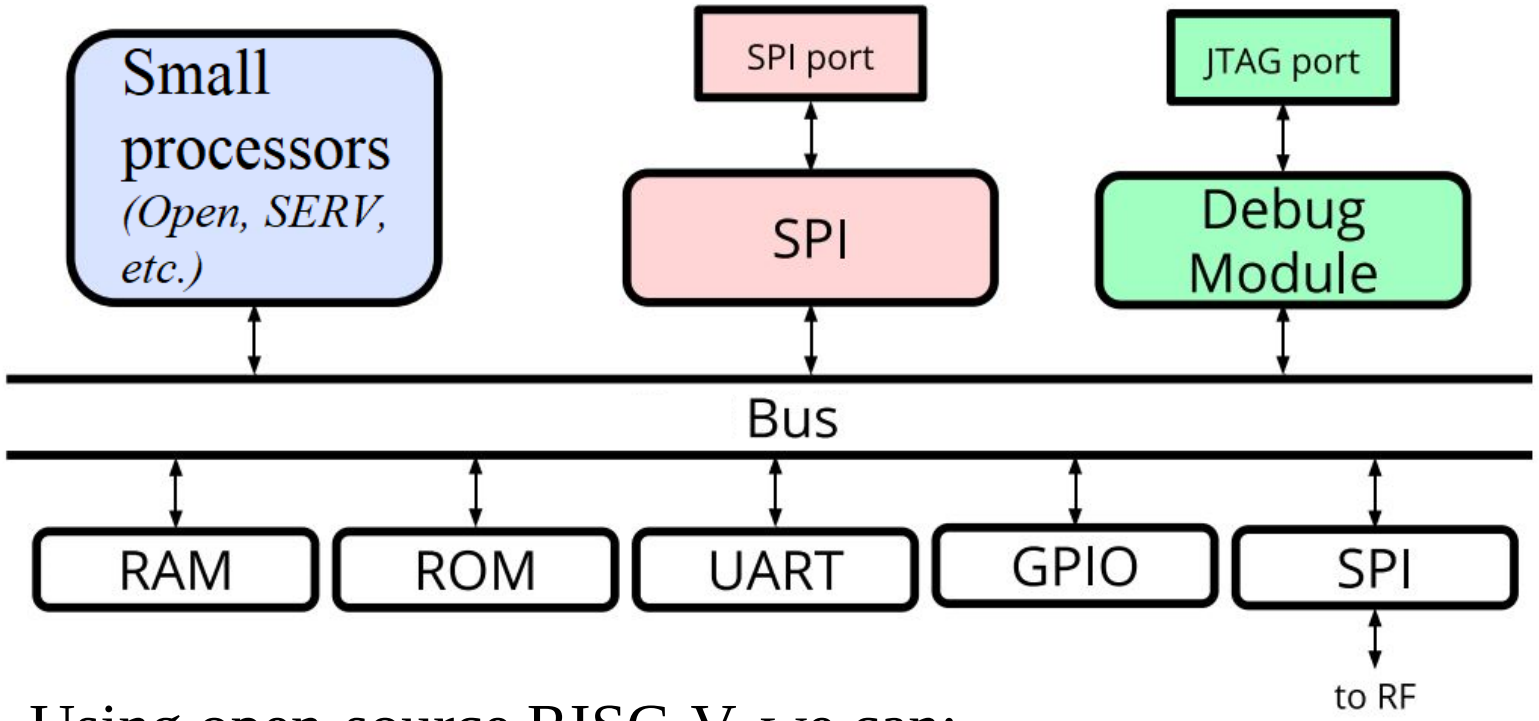
Depending on the technology, but a few μWs power supply are well in the range.

→ **Goal:** a complete SoC solution for self-powered IoT nodes

Source: *IEEE Access* (2021) [2]

2. Ultra-low-power SoC (4/8) Modular IoT-SoC

Issue #1: modular IoT-SoC architecture based on RISC-V



Open-source modular framework aiming for:

- Highly customizable
- Flexible and portable
- Wide range of applications

Using open-source RISC-V, we can:

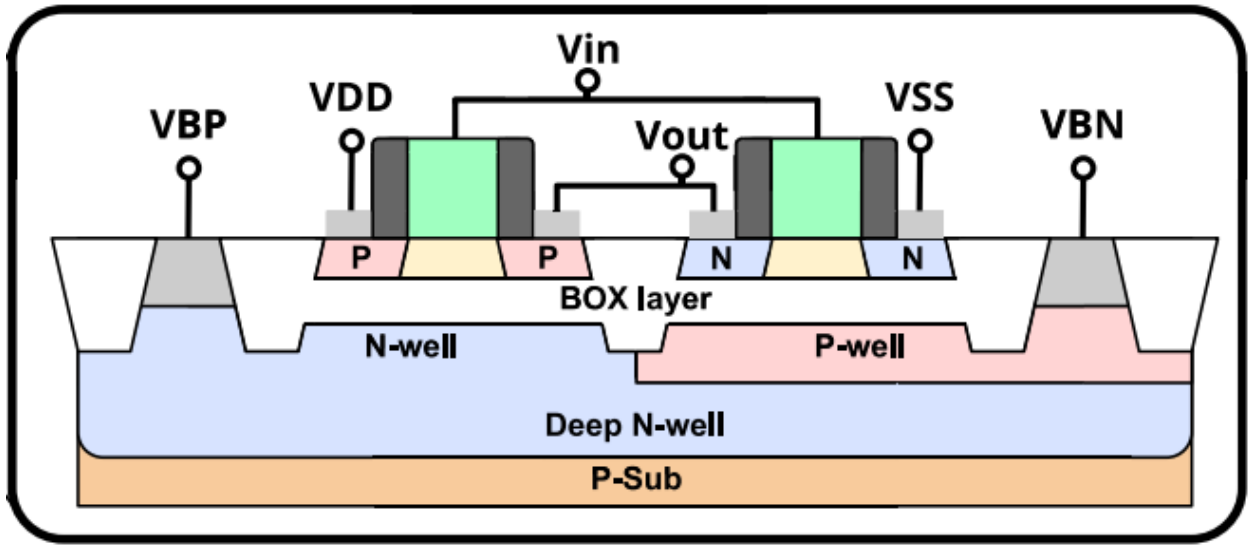
- Cheery-pick the wanted ISA extensions.
- Multiple options for the core processor(s) with wanted features *(i.e., low-power, high-performance, and security)*.
- Easy to develop & debug software.
- Vast options of peripherals: open sources, commercial IPs, in-house developments.

2. Ultra-low-power SoC (5/8) FD-SOI process

Issue #2: using Fully Depleted Silicon On Insulator (FD-SOI) processes

FD-SOI technology allows:

- Reducing leakage currents significantly
- Back-gate biasing technique
  - ❑ Apply reverse bias → even more power consumption reduces



SOTB-65nm (source: *TCAS-II*,2021 [3])

Combines a small MCU with FD-SOI
→ sub-μW SoC is well in the realm of reality

Energy harvesters (source: *IEEE Access*,2021 [2]):

- Solar sources: 1s mW/cm^2
- Electromagnetic sources: 100s μW/ cm^2

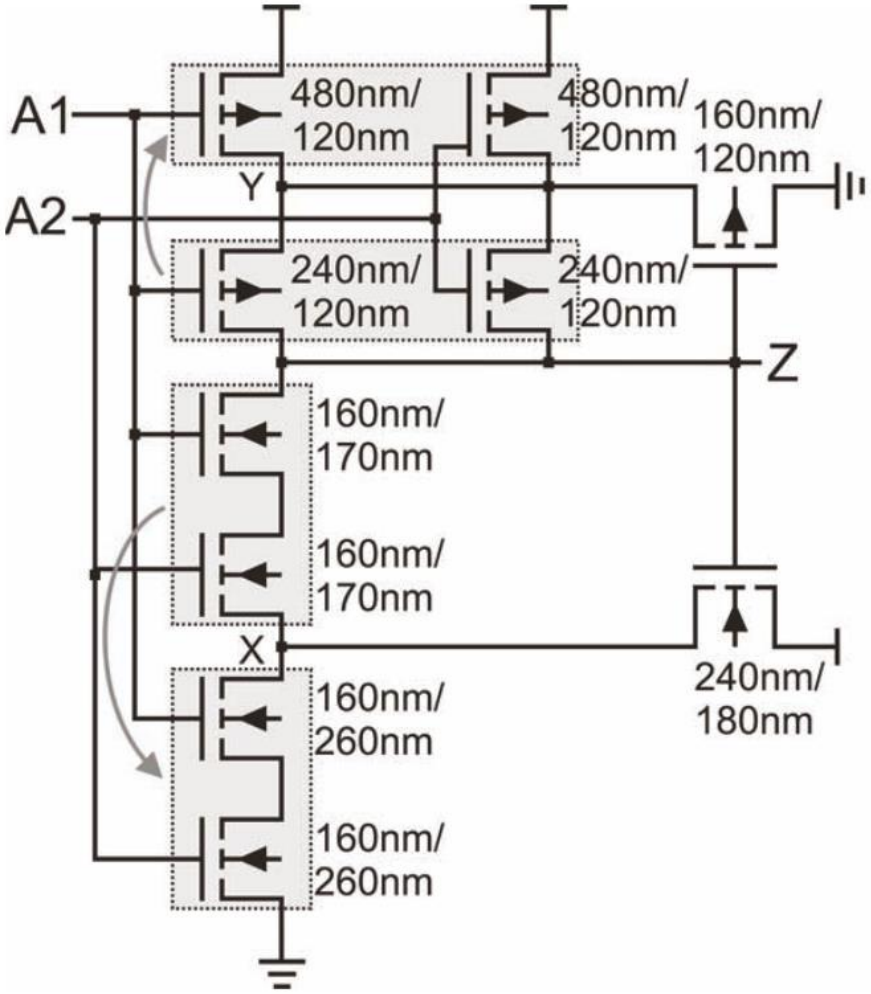
⇒

A sub-µW SoC will provide a comfortable room for the RF and sensing circuits.
→ Closing the gap toward wireless & battery-less IoT edge nodes.

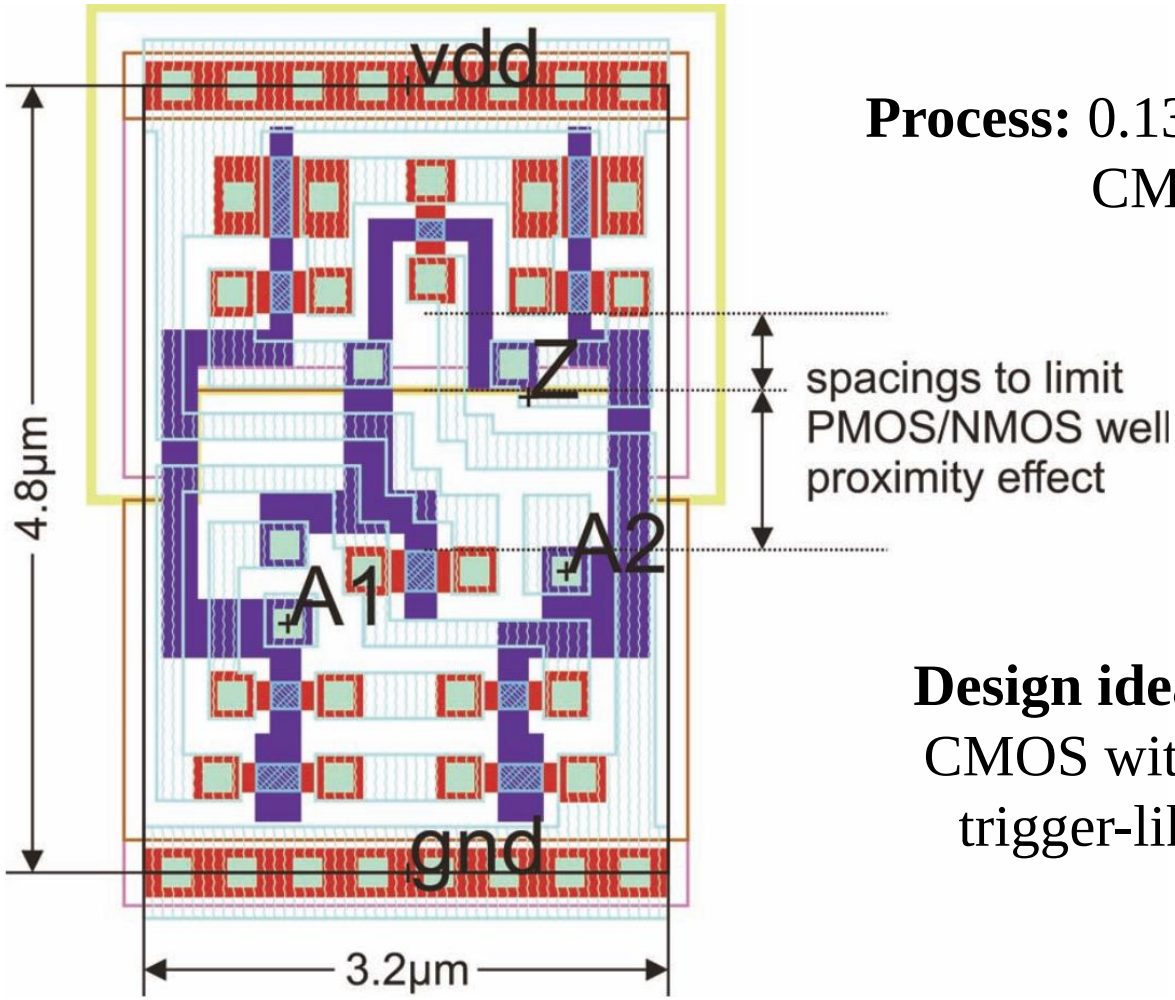
2. Ultra-low-power SoC (6/8) ULP StdCell

Issue #3: Ultra-Low-Power (ULP) standard cell

Design a ULP standard cells library: intentionally trade-off F_{Max} for low power



Schematic of the NAND2 gate



Layout of the NAND2 gate

Process: 0.13μm standard CMOS

Design idea: standard CMOS with Schmitt-trigger-like design

Source: *ISSCC* (2011) [4]

2. Ultra-low-power SoC (7/8) RF module

Issue #4: Ultra-Low-Power (ULP) RF transceiver & communication protocol

- Traditional IoT networks used existing cellular networks:
  LTE-M, NB-IoT, LPWAN, and WiFi.
  → Nowadays, short-range Bluetooth Low Energy (BLE) &
  Long Range radio (LoRa) are better for IoT.

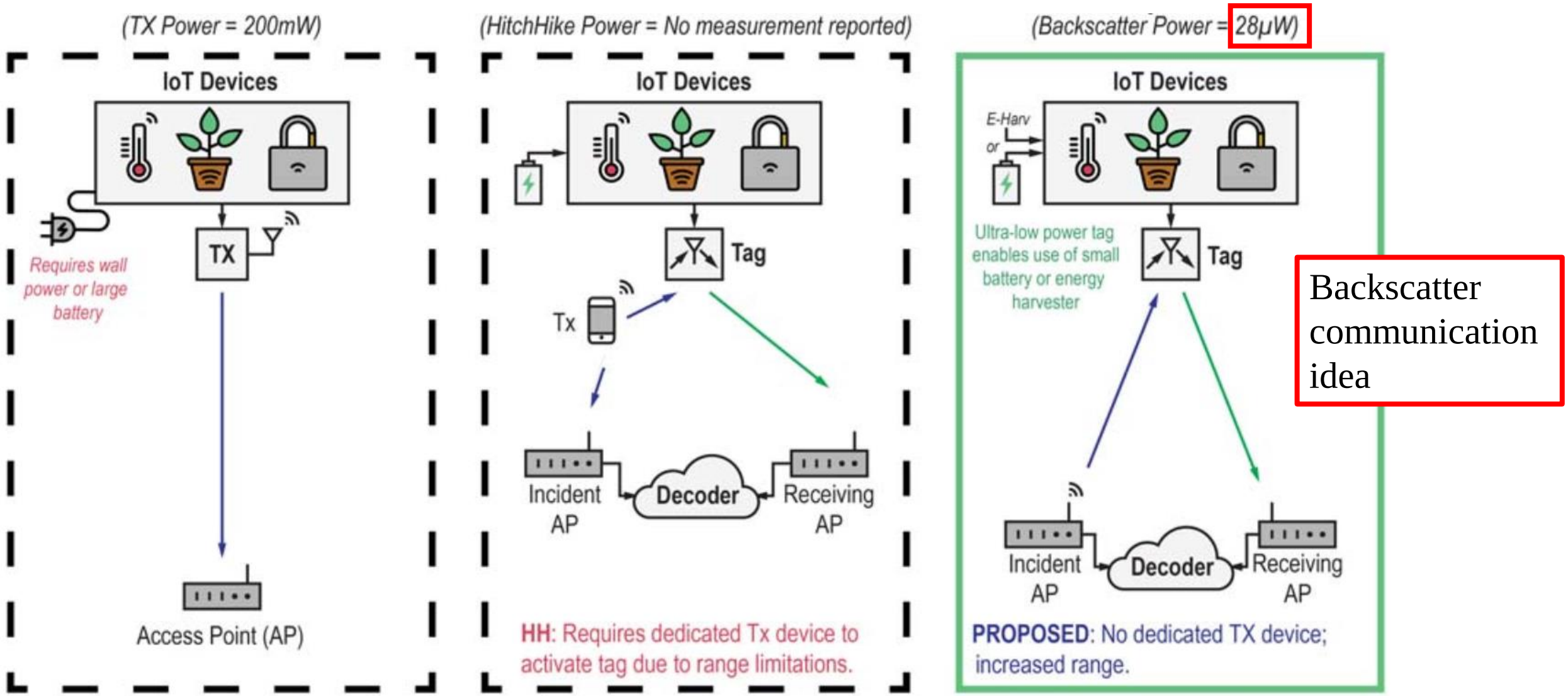
- Best attempts in reducing RF power consumption (source: *MOCAST*, 2018 [5]):
  - ❑ Receiver: 1s to 10s mW
  - ❑ Transmitter: 10s to 100s mW

  → Transceivers are easily in the range of mWs,
  with transmitters consuming about 5× to 10× more than a receiver.

- Propose a solution:
  Just ditch the transmitter and use a different approach for communications
  → The goal is to bring the transceiver module down to the range of μWs
  (source: *ISSCC*, 2020 [6])

2. Ultra-low-power SoC (8/8) RF module

Issue #4: Ultra-Low-Power (ULP) RF transceiver & communication protocol



[6] *ISSCC* (2020)

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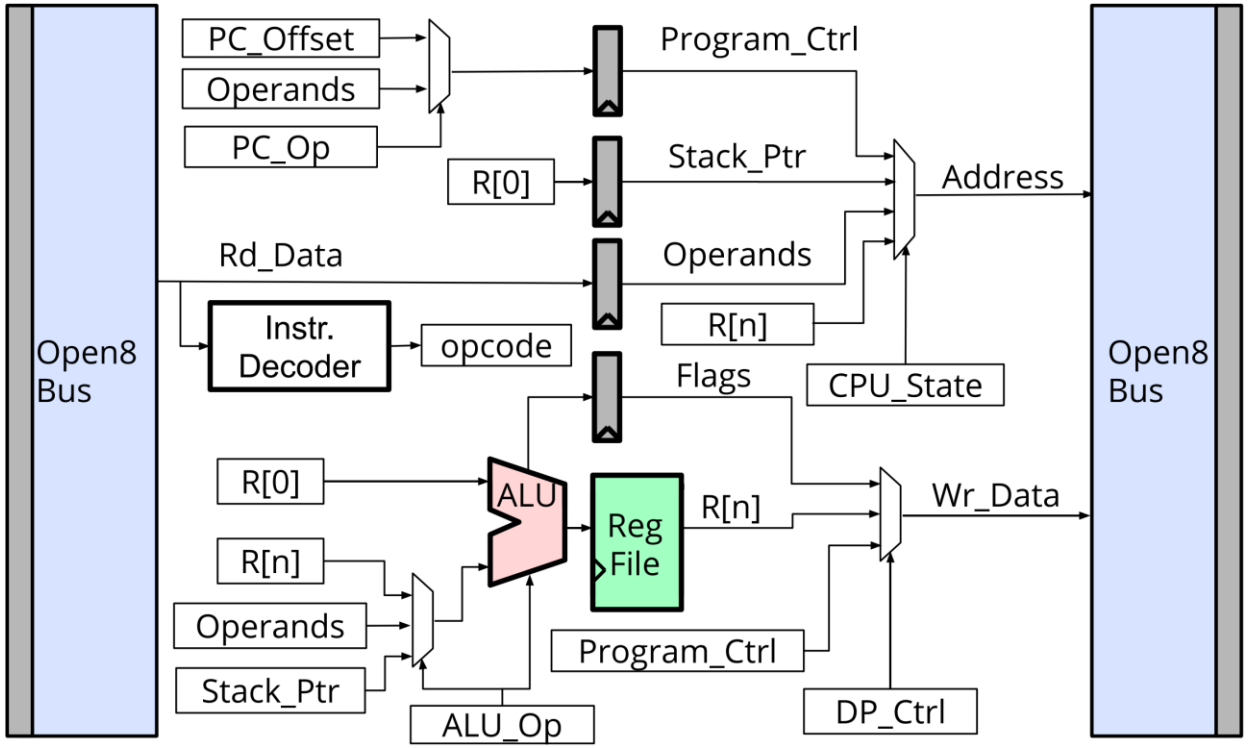
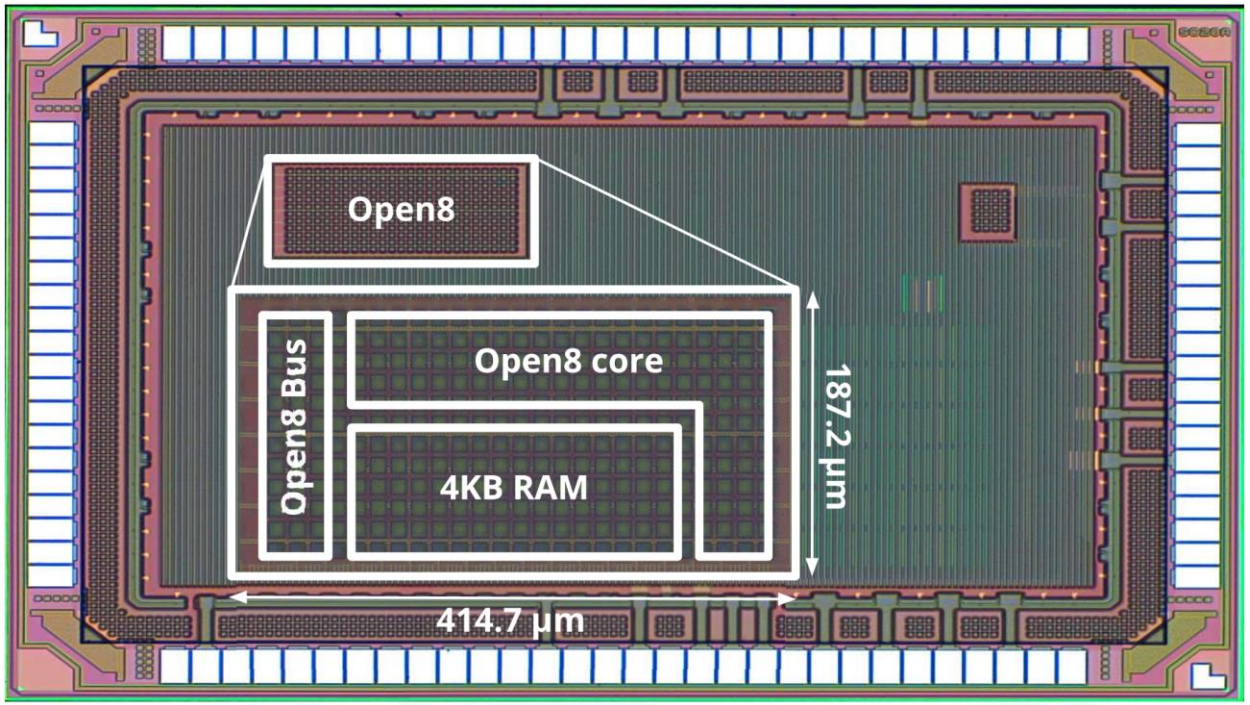
3. Our attempts (1/6) Open8: 8-bit MCU

Experiment with small MCUs:

try to achieve sub-µW power consumption



Open8 core data-path



Open8 in SOTB-65nm

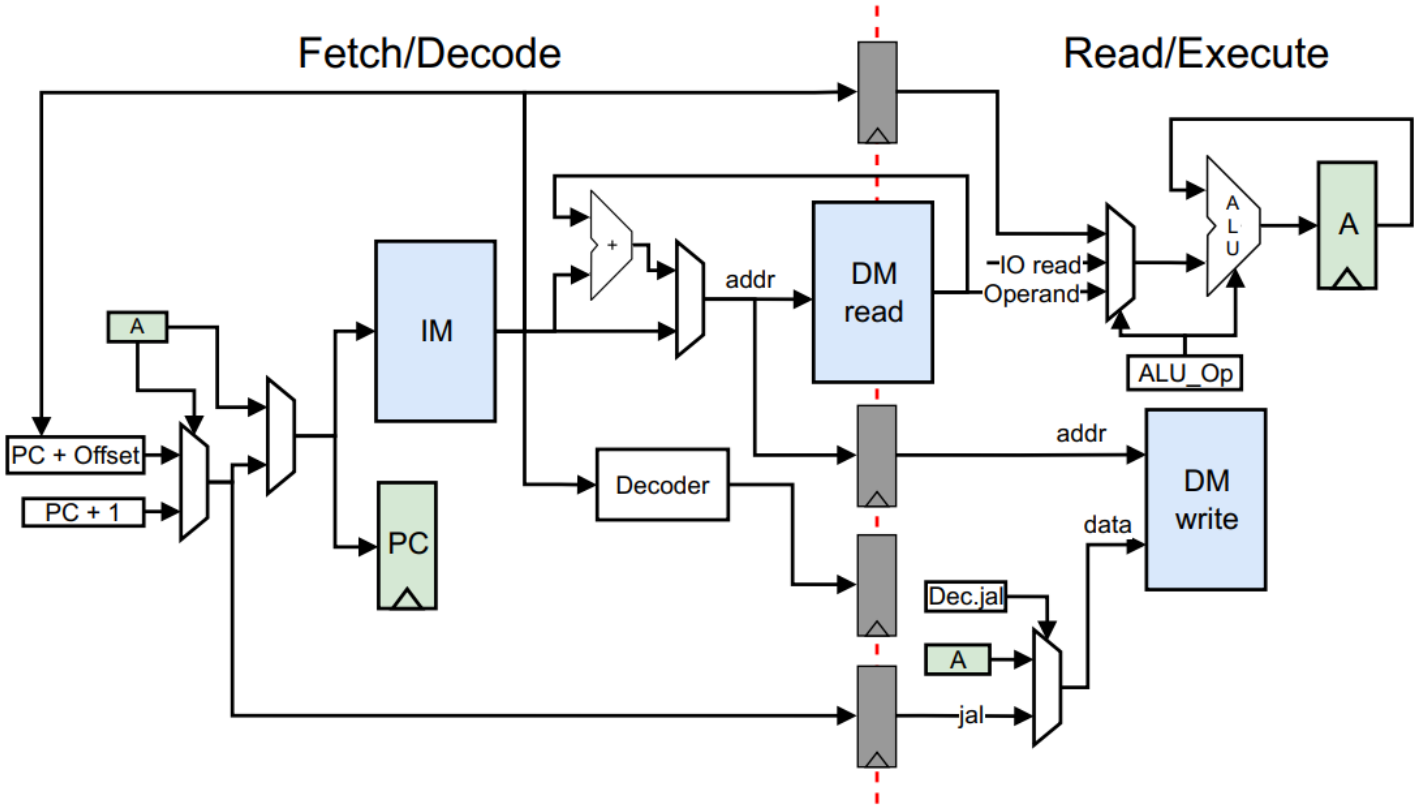
8-bit RISC processor

Open8 in *TCAS-II* (2021) [3]

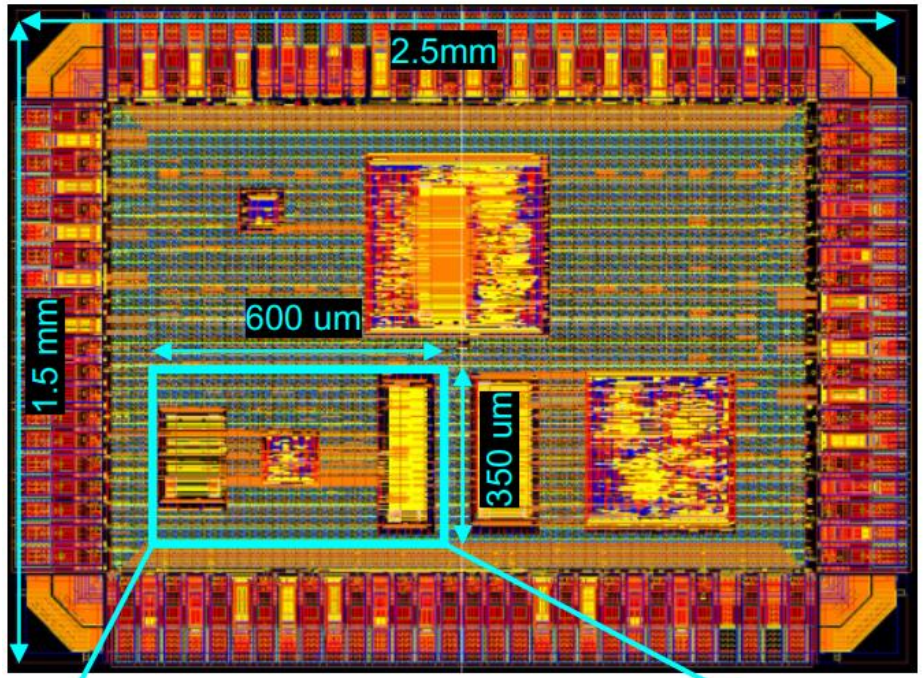
3. Our attempts (2/6) Leros: 16-bit MCU

Experiment with small MCUs:

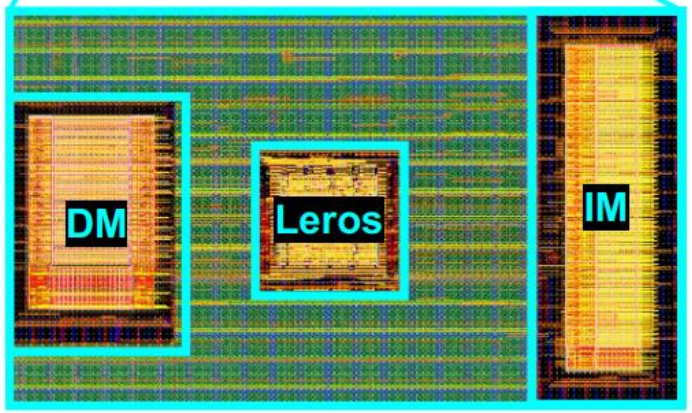
try to achieve sub-µW power consumption



Leros core data-path



Leros in SOTB-65nm



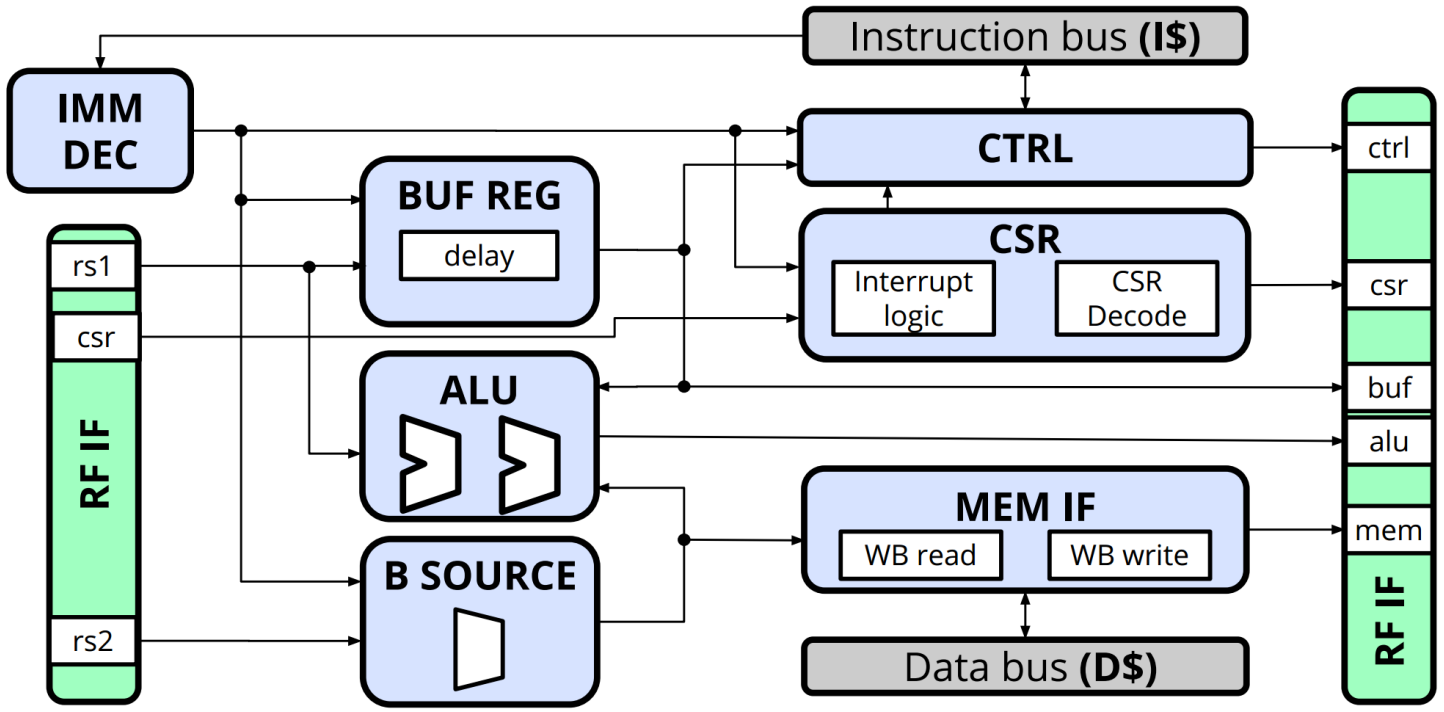
16-bit RISC processor

Leros in *ICICDT* (2022) [7]

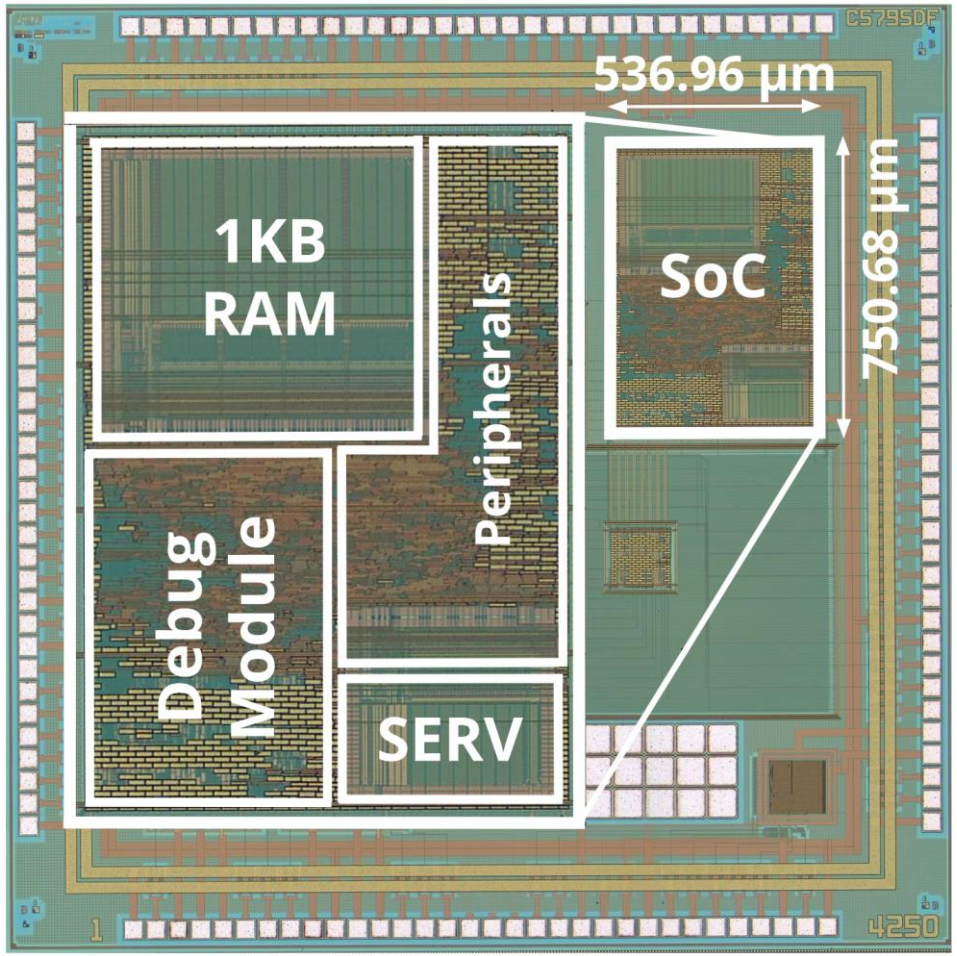
3. Our attempts (3/6) SERV: 32-bit *serial* MCU

Experiment with small MCUs:

try to achieve sub-µW power consumption



SERV core data-path



SERV in ROHM-180nm

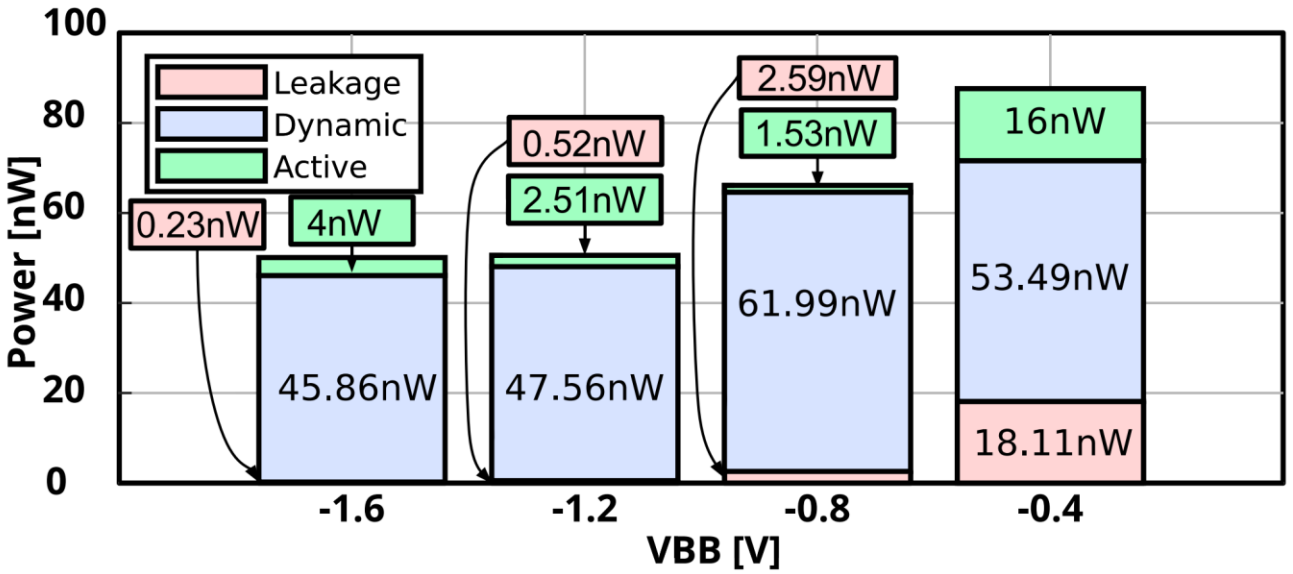
32-bit RISC-V serial processor

SERV in *ISOCC* (2021) [8]

3. Our attempts (4/6) Highlight key measurements

Experiment with small MCUs:

try to achieve sub-µW power consumption

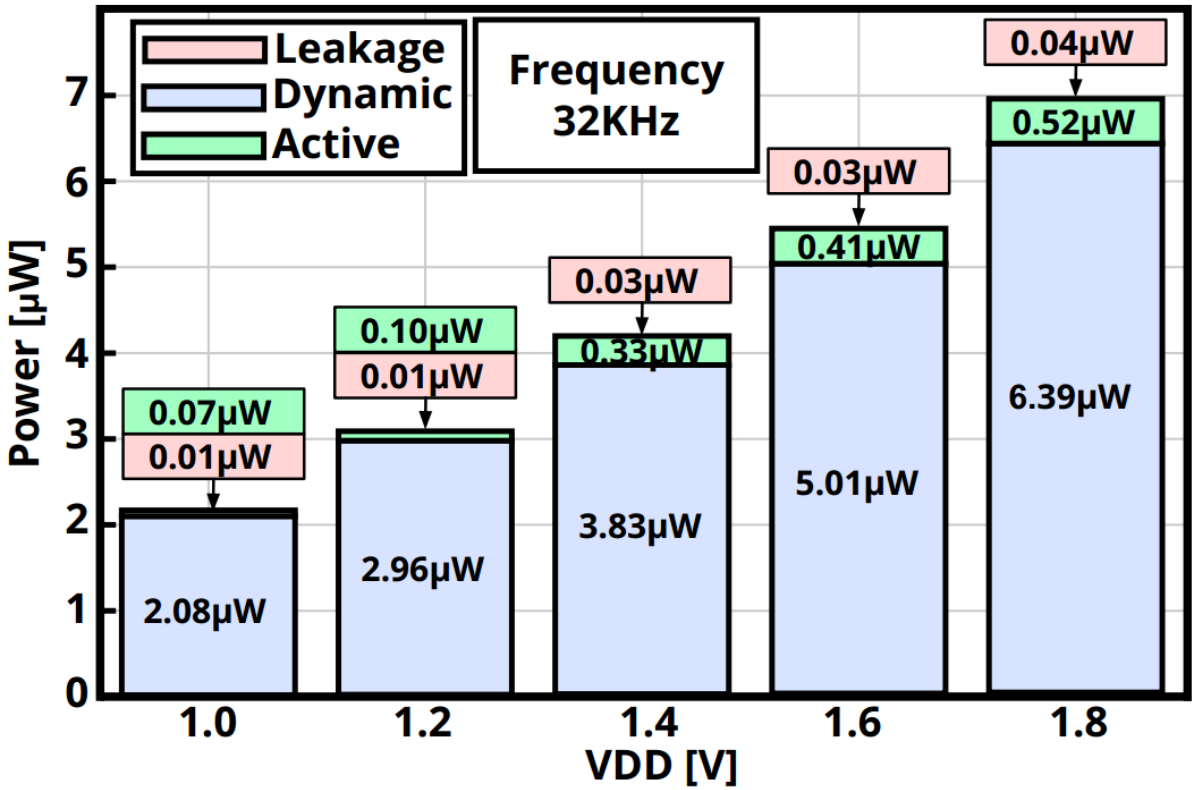


Open8 in SOTB65

(fixed V_{DD}=0.5-V & F=32-KHz)

Best P = 46.13nW *@V_{DD}=0.5-V,*

V_{BB}=−1.6-V & F=32-KHz



SERV in ROHM180nm

Best P = 2.16µW

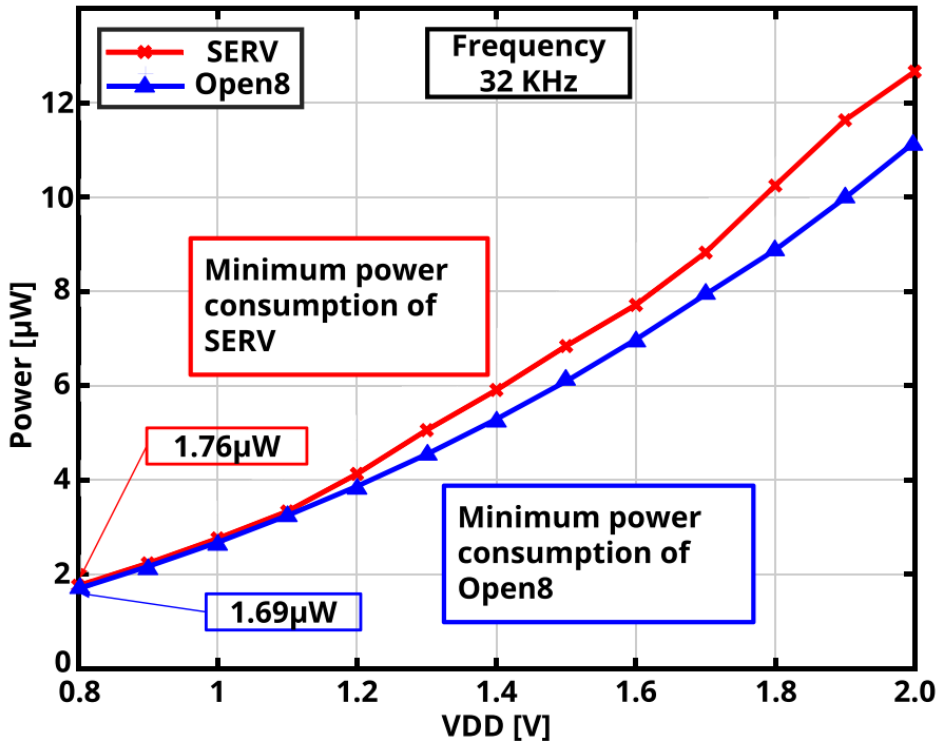
@V_{DD}=1.0-V & F=32-KHz

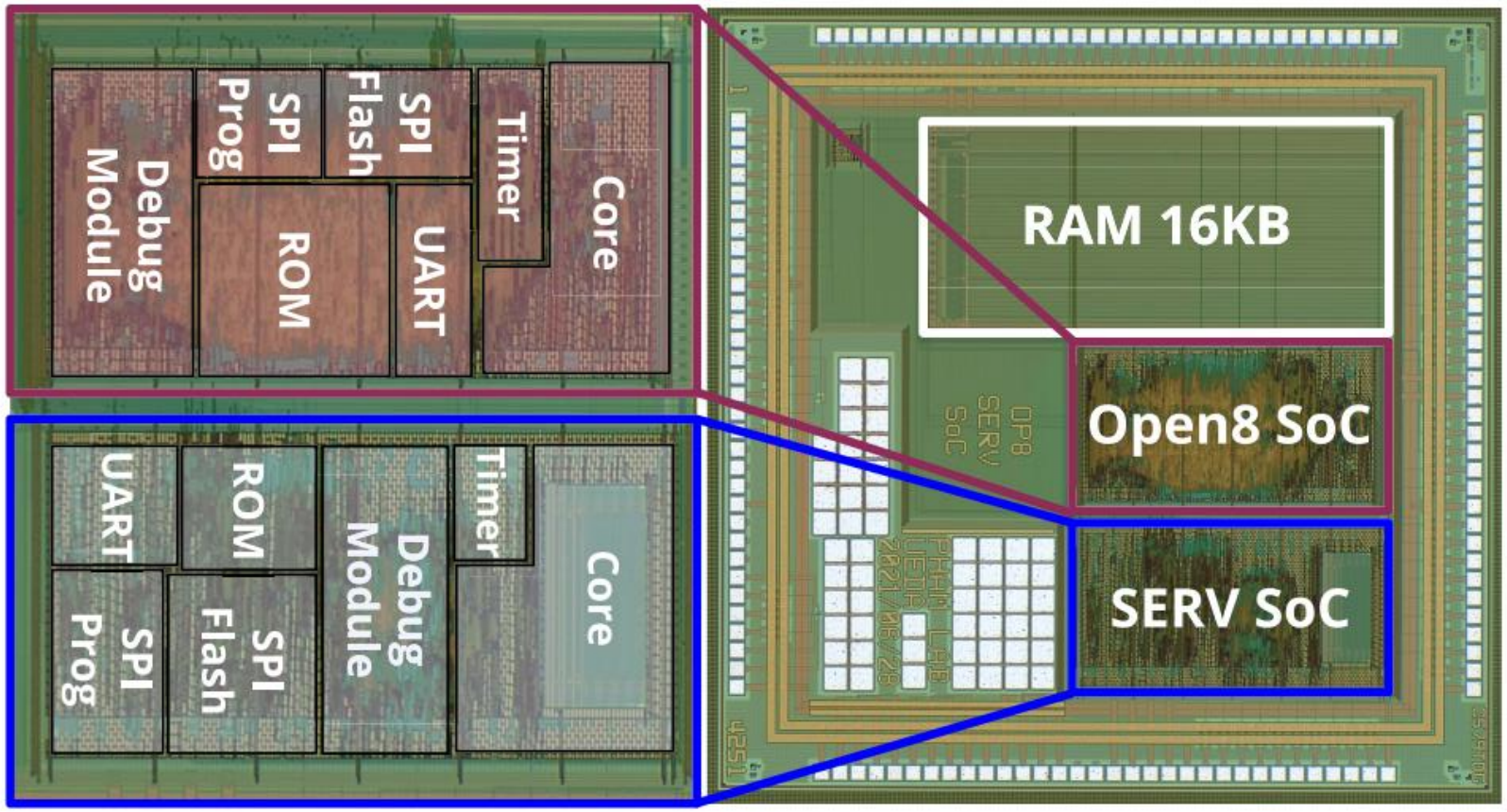
Open8 in *TCAS-II* (2021) [3] SERV in *ISOCC* (2021) [8]

3. Our attempts (5/6) Open8 + SERV

Experiment with small MCUs:
try to achieve sub-µW power consumption

The dual-core of Open8 & SERV in this chip is just for comparison fairness.

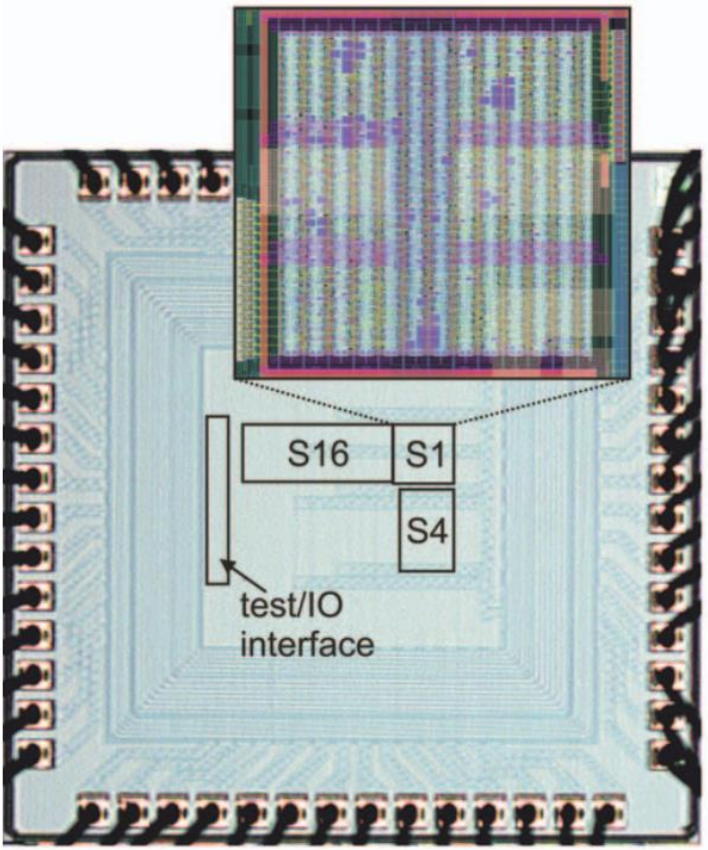




Open8+SERV in ROHM-180nm

Open8+SERV in *TCAS-II* (2022) [9]

2. Ultra-low-power SoC (6/6) What if: Open8 + ULP StdCell?



Source: *ISSCC* (2011) [4]

Process		0.13μm 8-metal CMOS
Design		8x8 Multiplier
Area (S1/S4/S16)		19176/23978/45002μm²
Supply Voltage (S1/S4/S16)		min. 84/68/62mV max. 1.2V
Minimum Energy/Operation Point		
Frequency	S1	544.8kHz@260mV
	S4	328.3kHz@233mV
	S16	210.1kHz@226mV
Power	S1	346.6nW@260mV
	S4	243.8nW@233mV
	S16	275.6nW@226mV
Energy/ Operation	S1	0.63pJ@260mV
	S4	0.74pJ@233mV
	S16	1.31pJ@226mV
Minimum Supply Voltage		
Frequency	S1	15.20kHz@84mV
	S4	10.35kHz@68mV
	S16	5.15kHz@62mV
Power	S1	29.9nW@84mV
	S4	21.1nW@68mV
	S16	17.9nW@62mV
Energy/ Operation	S1	1.97pJ@84mV
	S4	2.04pJ@68mV
	S16	3.48pJ@62mV

509.6pW/MHz-GE@0.26-V

⇩

Scaling equations in *Integration* (2017) [10]

⇩

345.14pW/MHz-GE @0.5-V *(SOTB65 no bias)*

⇩

Open8 [26] *(9kGE)*	SOTB-65nm: 99.4nW @0.5-V no bias & 32-KHz
SERV [27] *(2kGE)*	SOTB-65nm: 22.09nW @0.5-V no bias & 32-KHz

**Note:* ~10× more power reduction when a reverse bias is applied.

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4. Conclusion (1/1)

Toward the final goal of wireless self-powered IoT edge computing

1. A complete modular IoT-SoC framework will significantly reduce the R&D time.
2. FD-SOI processes should be used for ULP SoC.
3. ULP StdCell and RAM libraries should be developed with a specific mindset for IoT applications.
4. A ULP RF transceiver should be developed to reduce the total power consumption of an IoT edge node.

Ultra-low-power but also secure?

- The heavier the cryptographic functions, the better the security.
  → But that goes the opposite direction of an ideal IoT edge application.
- Therefore, ULP + Secure SoC design is the key direction that we are heading to.

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